CBCS Scheme

USN | | | | | | | | | | |

15ELN15/25

First/Second Semester B.E. Degree Examination, June/July 2016
Basic Electronics

Time: 3 hrs. Max. Marks: 80

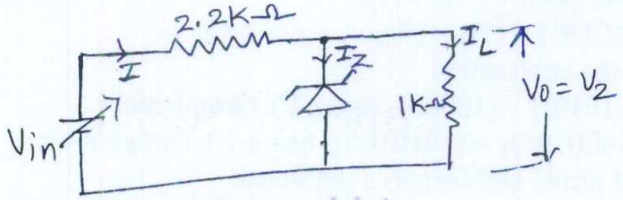
Note: ***Answer any FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the operation of pn junction diode under forward and reverse bias condition. **(06 Marks)**

b. For a zener regulator shown in the Fig.Q.1(b), calculate the range of input voltage for which output will remain constant.

Fig.Q.1(b)



$V_z = 6.1V$, $I_{z_{min}} = 2.5$ mA, $I_{z_{max}} = 25$mA, $r_z = 0\Omega$. **(04 Marks)**

c. Sketch the transistor input and output characteristics of CE configuration and briefly explain the three regions of operation. **(06 Marks)**

OR

2 a. With circuit diagram, explain the operation of center-tapped full-wave rectifier. Draw input and output waveforms. **(06 Marks)**

b. Explain how zener diode can be used as voltage regulator. **(05 Marks)**

c. Derive the relationship between α and β. Find the values of β, α and I_E for a transistor has $I_B = 100\ \mu A$ and $I_C = 2mA$. **(05 Marks)**

Module-2

3 a. With neat circuit diagram, explain the operation of voltage divider bias circuit with necessary equations. **(06 Marks)**

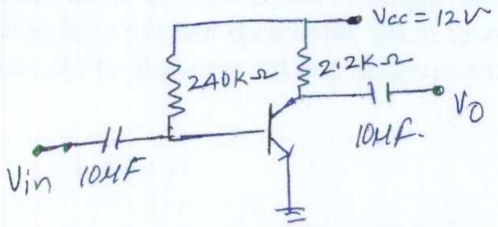
b. Draw the circuit of op-amp integrator. Derive the expression for output voltage. **(06 Marks)**

c. Calculate the o/p voltage of a three input inverting summing amplifier, given $R_1 = 200K\Omega$, $R_2 = 250K\Omega$, $R_3 = 500K\Omega$, $R_f = 1M\Omega$, $V_1 = -2V$, $V_2 = -1V$ and $V_3 = +3V$. **(04 Marks)**

OR

4 a. For the circuit shown in Fig.Q.4(a) find the Q-point values and draw DC-load line, where $V_{BE} = 0.7V$ and $\beta = 50$. **(06 Marks)**

Fig.Q.4(a)



b. Draw the circuit of non-inverting op-amp. Derive the expression for the voltage gain. **(05 Marks)**

c. Define the following terms with respect to op-amp: i) slew rate; ii) CMRR; iii) PSRR. **(05 Marks)**

Module-3

5 a. Convert:
i) $(526.44)_8 = (?)_2 = (?)_{10}$
ii) $(48350)_{10} = (?)_{16} = (?)_8$ **(04 Marks)**

b. Subtract the following using 2's complement method:
i) $101011_{(2)}$ from $111001_{(2)}$
ii) $111001_{(2)}$ from $101011_{(2)}$ **(04 Marks)**

c. Simplify the following expression and realize using basic gates:
$Y = A\left(\overline{ABC} + A\bar{B}C\right)$. **(04 Marks)**

d. Realize half adder using NAND gates only. **(04 Marks)**

OR

6 a. Convert:
i) $(342.56)_{10} = (?)_2 = (?)_8$
ii) $(BCDE) = (?)_2 = (?)_8$ **(04 Marks)**

b. Perform the subtraction
i) $(11010)_2 - (10000)_2$ using 1's complement.
ii) $(1000100)_2 - (1010100)_2$ using 2's complement. **(04 Marks)**

c. State and prove DeMorgan's theorems. **(04 Marks)**

d. Write the symbol, truth table and final expression for NAND and Ex – OR gate (For two I/PS). **(04 Marks)**

Module-4

7 a. With diagram and truth table explain NAND gate latch. **(05 Marks)**

b. With diagram and truth table explain clocked R-S flip-flop. **(05 Marks)**

c. Explain the architecture of 8051 microcontroller. **(06 Marks)**

OR

8 a. What is flip-flop? Explain the operation of NOR gate latch using its truth table. **(08 Marks)**

b. With block diagram, explain microcontroller based stepper motor control system. **(08 Marks)**

Module-5

9 a. With the help of block diagram, explain communication system. **(06 Marks)**

b. With circuit diagram explain the process of AM demodulation. **(05 Marks)**

c. Explain the principle of operation of piezoelectric transducer. **(05 Marks)**

OR

10 a. Why modulation is necessary in communication system? List the different types of modulation schemes. **(05 Marks)**

b. A carrier of 1MHz, with 400 W of its power is amplitude modulated with a sinusoidal signal of 2500Hz. The depth of modulation is 75%. Calculate the sideband frequencies, the band width, the power in the side bands and the total power in the modulated wave. **(05 Marks)**

c. Explain the construction and the principle of operation of LVDT. **(06 Marks)**

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